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EXAMINER	
LOHN, JOSHUA A	

ART UNIT	PAPER NUMBER
2114	5

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/775,496	Applicant(s) ZILBERMAN, EUGENE
	Examiner Joshua A Lohn	Art Unit 2114

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5 and 7-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5 and 7-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED FINAL REJECTION

Response to Arguments

Applicant's arguments filed 1/21/2004 have been fully considered but they are not persuasive. With respect to the applicant's arguments relating to claims 3 and 6, now incorporated within the limitations of claims 1 and 4, the examiner respectfully disagrees. The basis of the argument is that one of ordinary skill in the art at the time of the invention would not have found any motivation to use the invention of Jeddeloh in a system in which the primary memory is non-volatile. The examiner agrees that Jeddeloh teaches of a system in which the primary memory is a volatile memory. The examiner respectfully disagrees that the system would not obviously be used in conjunction with the inventions of Ajanovic and Okaue. All three systems teach of similar memory system structures, as is shown in the rejection of claim 1 below. It would have been obvious to one of ordinary skill in the art to that a non-volatile primary memory in the system would be desirable and compatible. This would have been obvious because a non-volatile memory is well known in the art to provide improved fault tolerance and reliability to the system, both of which are desirable. This would also been obvious because Jeddeloh comments on the compatibility of volatile and non-volatile memories, see column 3, lines 41-45, in reference to the to the storage of the memory controller. This compatibility could apply the same level of permanence to the primary storage, as is shown to be desirable above.

Applicant's arguments with respect to claims 9-11 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4, 5, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ajanovic, United States Patent number 6,298,426, filed December 31, 1997, in view of Jeddeloh, United States Patent number 6,052,798, filed July 1, 1998, in further view of Okaue et al., United States Patent number 6,601,140, filed April 6, 2000.

As per claim 1, Ajanovic discloses at least one main board that includes a processing system for enabling interaction with the host system, see Memory Controller (104) of figure 2. Ajanovic also discloses at least one memory board separate from the main board, with the memory board containing at least part of the storage systems primary solid-state component array used for data storage, see Memory Modules (200 A-D) of figure 2, which are independent boards that make up the solid-state memory for data storage, see column 4, lines 51-61. Ajanovic also discloses for each memory board having at least one secondary non-volatile memory device, located on the memory board, containing system information related to each memory board, see column 3, lines 61-66, where the NVRAM contains system information. Ajanovic fails to disclose the non-volatile memory containing fault location record for the primary solid-state components array located on the board. Ajanovic also fails to disclose the primary solid-state components being non-volatile.

Jeddeloh discloses using a secondary non-volatile memory to store a fault location record for the primary solid-state components array located on the board, see element 18 of figure 1 and column 3, lines 1-3.

It would have been obvious to one skilled in the art at the time the invention was made to include the fault location record of Jeddeloh in the memory module of Ajanovic.

This would have been obvious because Ajanovic discloses a memory module that contains a non-volatile memory for storing system information, as mentioned above. Jeddeloh discloses that including a fault map in a non-volatile secondary memory of a memory module allows for eliminating the need for redundant rows and extra bits for error correction schemes, see column 1, line 40 through column 2, line 4. It would be obvious to implement the fault map in the non-volatile memory of Ajanovic to eliminate this high memory overhead and still allow for detection and avoidance of faulty memory cells. Ajanovic and Jeddeloh fail to disclose the primary solid-state components being non-volatile memory.

Okaue discloses a memory module with a non-volatile primary solid-state memory component, see column 4, lines 48-50.

It would have been obvious to one skilled in the art at the time the invention was made to include the memory type of Okaue with the memory module of Ajanovic and Jeddeloh.

This would have been obvious because Ajanovic discloses a desire to have compatibility with different types of memory modules, see column 3, lines 34-40. Ajanovic and Jeddeloh both disclose a system in which each memory module has a primary and secondary segment, with the secondary segment responsible for storing information about the primary segment, as shown above. Okaue also adopts this form for a memory module, with a primary segment, element 42,

and a secondary information segment, the security block of element 52, both of figure 1. Due to the same memory structure of the modules it would have been obvious to one skilled in art at the time of the invention to allow for the memory module of Okaue, with its non-volatile primary memory block, to be used with the device of Ajanovic and Jeddeloh, which is shown to teach of compatibility with different memory modules.

As per claim 2, Ajanovic discloses a memory board including at least a portion of the primary solid-state components array, see column 4, lines 61-61, where the for memory boards, or modules, make up the primary solid-state memory. Ajanovic also discloses at least one respective secondary non-volatile memory device containing system information related to the main board, see column 3, lines 63-66, which describe the system information stored on the secondary non-volatile memory.

As per claim 4, Ajanovic discloses placing a secondary non-volatile memory device onto each board of the multi-board solid-state storage system, see elements 201 A-D of figure 2. Ajanovic discloses recording system information of each board on the secondary non-volatile memory device, see column 3, lines 64-66. Ajanovic fails to disclose the non-volatile memory containing fault location record for the primary solid-state components array located on the board. Ajanovic also fails to disclose the primary solid-state components being non-volatile.

Jeddeloh discloses using a secondary non-volatile memory to store a fault location record for the primary solid-state components array located on the board, see element 18 of figure 1 and column 3, lines 1-3.

It would have been obvious to one skilled in the art at the time the invention was made to include the fault location record of Jeddeloh in the memory module of Ajanovic.

This would have been obvious because Ajanovic discloses a memory module that contains a non-volatile memory for storing system information, as mentioned above. Jeddeloh discloses that including a fault map in a non-volatile secondary memory of a memory module allows for eliminating the need for redundant rows and extra bits for error correction schemes, see column 1, line 40 through column 2, line 4. It would be obvious to implement the fault map in the non-volatile memory of Ajanovic to eliminate this high memory overhead and still allow for detection and avoidance of faulty memory cells. Ajanovic and Jeddeloh fail to disclose the primary solid-state components being non-volatile memory.

Okaue discloses a memory module with a non-volatile primary solid-state memory component, see column 4, lines 48-50.

It would have been obvious to one skilled in the art at the time the invention was made to include the memory type of Okaue with the memory module of Ajanovic and Jeddeloh.

This would have been obvious because Ajanovic discloses a desire to have compatibility with different types of memory modules, see column 3, lines 34-40. Ajanovic and Jeddeloh both disclose a system in which each memory module has a primary and secondary segment, with the secondary segment responsible for storing information about the primary segment, as shown above. Okaue also adopts this form for a memory module, with a primary segment, element 42, and a secondary information segment, the security block of element 52, both of figure 1. Due to the same memory structure of the modules it would have been obvious to one skilled in art at the time of the invention to allow for the memory module of Okaue, with its non-volatile primary

memory block, to be used with the device of Ajanovic and Jeddeloh, which is shown to teach of compatibility with different memory modules.

As per claim 5, Ajanovic discloses that the memory modules can take on multiple, different organizations, see column 3, lines 33-42. This would inherently include the ability to add, connect, and replace boards to provide for the different organizations. Ajanovic also discloses testing the boards by providing error detection on the data retrieved from the memory boards, see column 5, lines 18-21.

As per claim 7, Okaue discloses the primary solid-state components are Flash memory devices, see column 4, lines 48-50.

As per claim 8, Okaue discloses the primary solid-state components are Flash memory devices, see column 4, lines 48-50

Claims 9, 10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ajanovic in view of Jeddeloh in further view of Gross et al., United States Patent number 5,200,959, filed October 17, 1989.

As per claim 9, Ajanovic discloses placing a secondary non-volatile memory device onto each board of the multi-board solid-state storage system, see elements 201 A-D of figure 2. Ajanovic discloses recording system information of each board on the secondary non-volatile memory device, see column 3, lines 64-66. Ajanovic fails to disclose the non-volatile memory containing fault location record for the primary solid-state components array located on the

board. Ajanovic also fails to disclose storing the information in each of at least two areas of the secondary memory.

Jeddeloh discloses using a secondary non-volatile memory to store a fault location record for the primary solid-state components array located on the board, see element 18 of figure 1 and column 3, lines 1-3.

It would have been obvious at the time the invention was made to include the fault location record of Jeddeloh in the memory module of Ajanovic.

This would have been obvious because Ajanovic discloses a memory module that contains a non-volatile memory for storing system information, as mentioned above. Jeddeloh discloses that including a fault map in a non-volatile secondary memory of a memory module allows for eliminating the need for redundant rows and extra bits for error correction schemes, see column 1, line 40 through column 2, line 4. It would be obvious to implement the fault map in the non-volatile memory of Ajanovic to eliminate this high memory overhead and still allow for detection and avoidance of faulty memory cells. Ajanovic and Jeddeloh fail to disclose storing faulty location information in each of at least two areas of the secondary memory.

Gross discloses storing faulty location information in each of at least two areas of a memory, see column 8, lines 52-56.

It would have been obvious to one skilled in the art at the time the invention was made to include the multiple fault location information lists of Gross in the invention of Ajanovic and Jeddeloh.

This would have been obvious because of the importance of the fault information in avoiding defects in memory. It is discloses by Jeddeloh that the list of defective memory

locations is essential to all aspects of the avoidance of faulty locations, see column 2, lines 7-38. Gross discloses that care must be taken to ensure that the defect list is kept accurately, and that a method for ensuring that the list does not become corrupted is to use redundant lists, see column 8, lines 35-56. It would have been obvious that the defect list, which is essential to the invention of Ajanovic and Jeddeloh, would have benefited greatly from being duplicated and stored in at least two areas of memory.

As per claim 10, Gross discloses redundant lists of defects, see column 8, lines 52-56. Jeddeloh discloses updating these lists subsequent to initial recording, see column 5, lines 9-34.

As per claim 11, Gross discloses redundant lists of defects, see column 8, lines 52-56. Jeddeloh discloses adding at least one additional fault location record to these lists, see column 5, lines 9-34.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure is provided on form PTO-892.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua A Lohn whose telephone number is (703) 305-3188. The examiner can normally be reached on M-F 8-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoleil can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAL

SCOTT BADERMAN
PRIMARY EXAMINER